CHV Series Vector Control Inverter Options

Operating Instructions for PG Card

1. Model and Specifications

1.1 Model Description

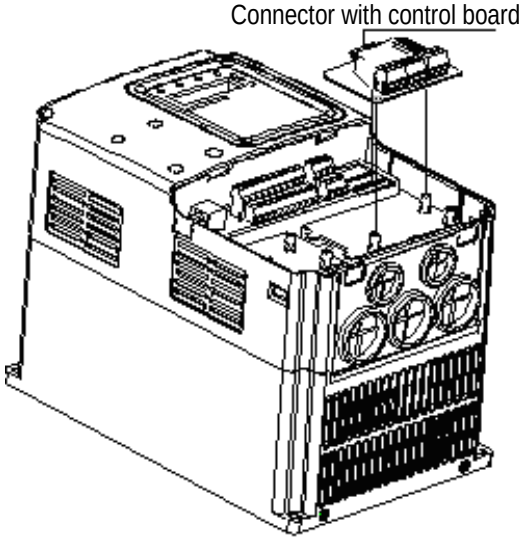
The model of PG card for CHV inverters is PN000PGWX.

1.2 Technical Features

	Function	Response Speed	Output Impedance	Voltage Range	Output Current	Frequency Division Range
+12V, COM1	Coder power supply	---	About 300Ω	12~16V	300mA	---
TERA+, TERA-, TERB+, TERB-	Coder signal access	0~80 KHz	---	0-24V	---	---
TER-OA, TER-OB	Frequency division signal output	0~80 KHz	About 30Ω	---	100mA	1~256 (even number)

1.3 Dimensions and Installation

Installation diagram of PG card



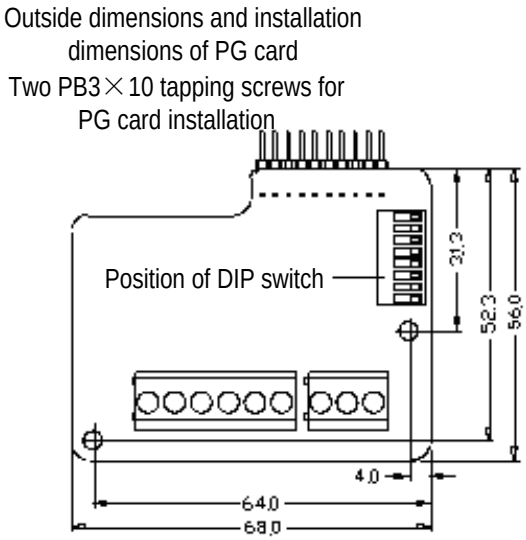


Figure 1.1 Installation and Dimensions of PG Card.

2. Operating Instructions

2.1 Functions

If the user requires PG vector control, need to select PG card. The function of the PG card includes processing circuits for two channels of orthogonal coder signals, capable of receiving signals from differential output, open-circuit collector output and push-pull output encoders. Coder power supply (+12V output, adjustable through the potentiometer on the PG card). In addition, it can output in frequency-division the inputted encoder signals (output are two channels of orthogonal signals). The user can make selection according to actual situations.

2.2 Description of Terminals and DIP Switch

The PG card has nine wiring terminals, as shown in Figure 2.1.

+12V	COM1	TERA+	TERA-	TERB+	TERB-

TER-OA	TER-OB	COM1

Figure 2.1 Wiring Terminals.

Where, +12V and COM1 are working voltage output for the coder; TERA+, TERA-, TERB+, and TERB- are signal input terminals for the coder; TER-OA, TER-OB, and COM1 are output terminals for frequency-division signals; PE is the wiring terminal for shielding cable (PE inside the PG card is not connected to the ground, and the user can connect it to the ground during use).

The frequency division factor is determined by the DIP switch on the card. The DIP switch consists of 8 bits. When the binary digits displayed by DIP switch pluses 1, the relative value is frequency division factor. The bit marked as “1” on the DIP switch is the lower binary bit,

while “8” is the higher binary bit. When the DIP switch is switched to ON, the bit is valid, indicating “1”; otherwise, it indicates “0”.

Frequency division factors are shown in the table below:

Decimal Digit	Binary Digit	Frequency Division Factor
0	00000000	1
1	00000001	2
2	00000010	3
…	…	…
m	…	m+1
255	11111111	256

2.3 Wiring Diagram

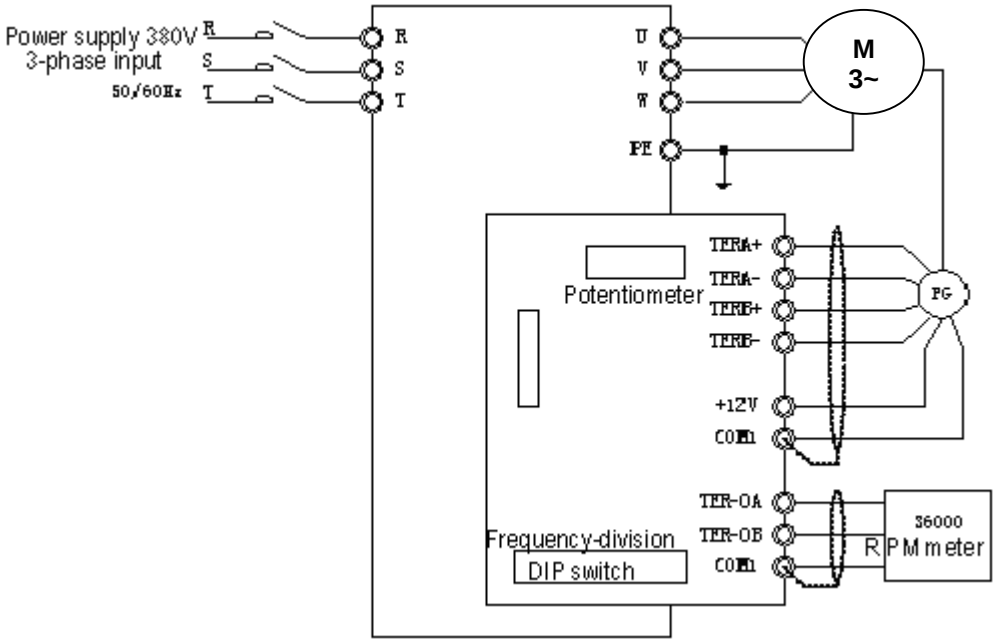


Figure 2.2 Wiring Diagram.

2.4 Precautions on Wiring

- The signal line of PG card should be separated from the power line. Parallel wiring is forbidden.
- To prevent coder signals from disturbance, please select a shielded cable as the signal line of PG card.
- The shielding layer of shielded cable of PG card should be grounded (such as terminal PE of the inverter), and furthermore, only one end is grounded, to prevent signal from disturbance.
- If the frequency-division output of PG card is connected to user power supply, the voltage

should be less than 24V; otherwise, the PG card may be damaged.

3. Application Connection

3.1 Wiring Diagram of Differential Output Coder

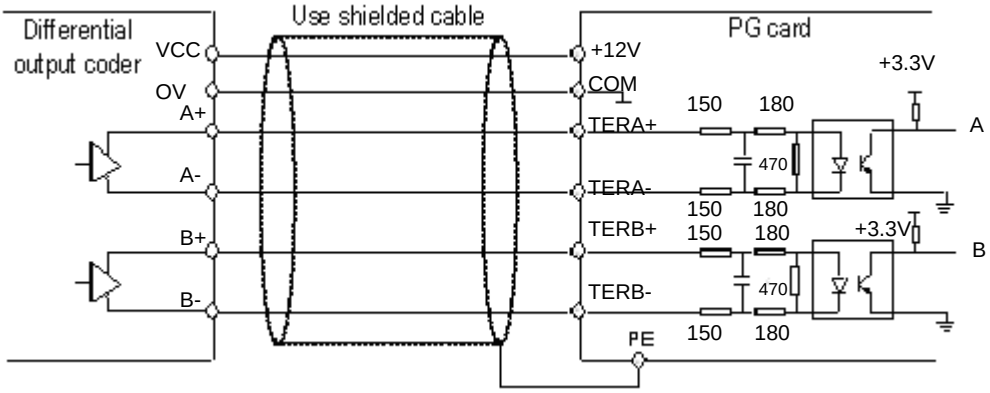


Figure 3.1 Wiring Diagram of Differential Output Coder.

3.2 Wiring Diagram of Open Collector Output Coder

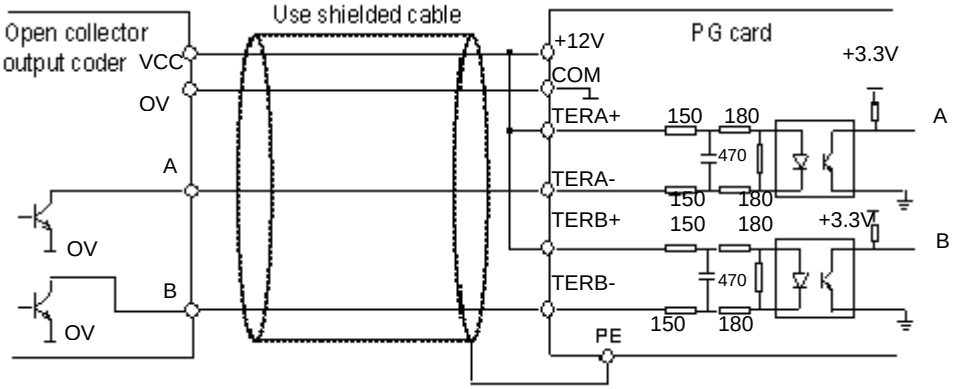


Figure 3.2 Wiring Diagram of Open Collector Output Coder.

3.3 Wiring Diagram of Push-pull Output Coder

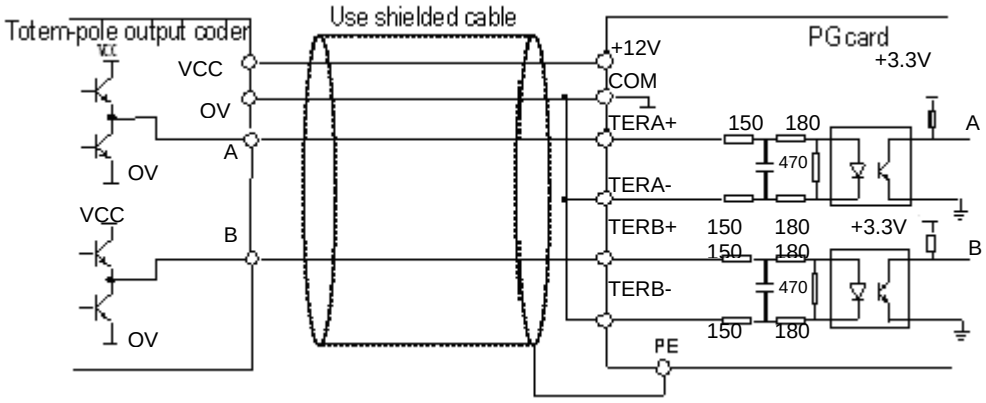


Figure 3.3 Wiring Diagram of Push-pull Output Coder.

3.4 Wiring Diagram of PG Card Frequency-division Output

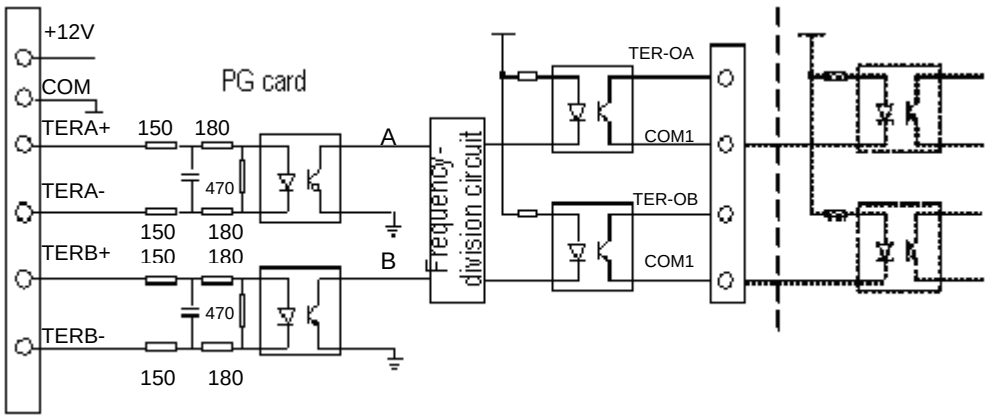


Figure 3.4 Wiring Diagram of PG Card Frequency-division Output.